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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
MCFADDEN, MICHAEL B	

ART UNIT	PAPER NUMBER
2188	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/783,376	BRAUN ET AL.	
	Examiner	Art Unit	
	Michael B. McFadden	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 February 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Request for Continued Examination

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12 February 2008 has been entered.

Status of Claims

2. Claims 1-22 are pending in the Application.

Response to Amendment

3. Applicant's arguments filed on 08 January 2008 have been fully considered but they are not persuasive.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made

to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Haupt (US Patent No. 6,334,159) and further in view of Halbert et al. ((US Patent No. 6,317,352) herein after Halbert).

6. **Regarding Claims 1, 16, and 22,** Haupt discloses a synchronous memory system **(Haupt: Column 7, Lines 2-4)**, comprising: a plurality of memory modules in a main memory **(Haupt: Figure 1, Elements 110A-D)**, with each memory module comprising at least two memory banks **(Haupt: Figure 2, Elements 535A, 535B, 535C, and 535D)**, a memory control device configured to generate commands comprising a plurality of command segments with a respective plurality of elements **(Haupt: Figure 1, Element 120A)**, wherein one of the command segments is a selection command segment for selecting at least two memory banks, and wherein each of the memory banks has at least one uniquely associated element of the selection command segment, and a transfer bus **(Haupt: Figure 1, Element 130 which includes Figure 2, Elements 510 and 520)** for communication between the memory control device and the memory modules, wherein the transfer bus comprises a plurality of parallel transfer lines; and wherein the memory control device is configured to transfer the commands to the memory modules using the transfer bus, and wherein the transfer bus is configured to transfer the elements of a command segment in parallel over the parallel transfer lines, **(Haupt: Column 5, Lines 40-51) It is noted that the POD has the capability to**

address one of the storage sub-units and therefore inherently possesses a selection command. (Haupt: Column 6, Lines 10-14.)

7. Haupt fails to disclose wherein the transfer bus is in the form of a daisy chain structure and wherein the daisy chain structure comprises a first point-to-point connection from the memory control device to a first memory module of the plurality of memory modules and a second point-to-point connection from the first memory module of the plurality of memory modules to a second memory module of the plurality of memory modules whereby the memory control device and the plurality of memory modules are interconnected to form a daisy chain.

8. Halbert discloses wherein the transfer bus is in the form of a daisy chain structure and wherein the daisy chain structure comprises a first point-to-point connection from the memory control device to a first memory module of the plurality of memory modules and a second point-to-point connection from the first memory module of the plurality of memory modules to a second memory module of the plurality of memory modules whereby the memory control device and the plurality of memory modules are interconnected to form a daisy chain. **(Halbert: Figure 4. Column 1, Lines 7-11. Column 4, Lines 15-50.)**

9. It would be obvious to one of skill in the art to combine the known technique of daisy chaining memory modules as taught in Halbert with the system of Haupt to achieve the predictable result of a serially connected memory module chain.

10. **Regarding Claims 2 and 17,** Haupt and Halbert disclose wherein each of the plurality of memory modules further comprises a buffer device for forwarding the

commands to at least two memory banks in at least one of a respective memory module of the plurality of memory modules and one or more other memory modules of the plurality of memory modules. **(Haupt: Figure 2, Elements 550 and 530)**

11. **Regarding Claims 3 and 18,** Haupt and Halbert disclose where the buffer device is configured to compare the bit pattern of a given selection command segment with one or more predetermined bit patterns and to determine whether the associated command needs to be forwarded to at least one of: (i) the at least two of the memory banks in the respective memory module, (ii) and the one or more other memory modules. **(Haupt: Column 6, Lines 10-14 and Lines 47-52)**

12. **Regarding Claims 4 and 19,** Haupt and Halbert disclose wherein the buffer device is configured to generate a chip select signal for the at least two memory banks. **(Haupt: Column 6, Lines 10-14 and Lines 44-52)**

13. **Regarding Claims 5 and 20,** Haupt and Halbert disclose where the selection command segment is the first segment of the commands. **The Office notes that the location of the select command is a design choice. Haupt Column 6, Lines 44-55 teaches that it queues memory requests and provides the appropriate requested address.**

14. **Regarding Claim 6,** Haupt and Halbert disclose wherein the number of transfer lines in the transfer bus is at least equal to the maximum number of memory banks which can be used in the memory system. **(Haupt: Figures 1 and 2)**

15. **Regarding Claims 7 and 8,** Haupt and Halbert disclose wherein the commands contain an element for a clock enable signal for all the memory banks. **(Haupt: Column 6, Lines 59-63, Column 10, Lines 17-19, and Column 11, Lines 44-56)**

16. **Regarding Claims 12 and 13,** Haupt and Halbert disclose wherein the commands contain an element for a reset signal and comprising a transfer line connecting the memory control device and at least one of the memory modules and configured to propagate a reset signal. **(Haupt: Column 6, Lines 55-59) The Flush command functions the same as a reset command.**

17. **Regarding Claim 14,** Haupt and Halbert disclose wherein the commands contain an element for signaling that the command is intended for the buffer device. **(Haupt: Column 6, Lines 47-52 and Lines 59-63) The control commands are intended for the buffer and indicate control information the buffer is to apply. Therefore the element to signal that the command is intended for the buffer must be inherent.**

18. **Regarding Claims 15 and 21,** Haupt and Halbert disclose wherein the memory control device comprises a coding device for coding generated commands and the buffer device comprises a decoding device for decoding received coded commands.**(Haupt: Figure 9, Element 1290) The inclusion of a decoding device points to the fact that commands must be decoded. Therefore the inclusion of an encoding device is inherent.**

19. **Regarding Claims 9, 10, and 11,** Haupt and Halbert fail to disclose the inclusion of an on-die termination signal.

20. The Office takes Official Notice that it would have been obvious to a person of ordinary skill in the art to include an on-die termination signal in the memory system of Haupt.

21. The motivation for doing so would have been to eliminate bouncing and ringing that occurs whenever a signal hits an interface in its path.

22. Therefore it would have been obvious to include an on-die termination signal in the memory system of Haupt in order to eliminate bouncing and ringing that occurs whenever a signal hits an interface in its path to obtain the invention as described in Claims 9, 10, and 11.

Response to Arguments

23. Applicant's arguments filed on 08 January 2008 have been fully considered but they are not persuasive.

24. **Regarding Claim 1,** the Applicant contends that Haupt fails to disclose a memory module and selection command that comprises at least two memory banks. **However, the rejection cites Figure 2, Elements 535A, 535B, 535C, and 535D as the memory modules. Each memory module (called a memory cluster (MCL)) contains 4 MSU expansions. Each expansion contains 2 storage arrays. Therefore, each memory module contains 8 memory arrays which is more than two, fulfilling the "at least two" requirement. Selecting one of the memory modules would select 8 of the arrays, therefore fulfilling the "at least two" requirement.**

25. Regarding all other Claims not specifically traversed above and whose rejections were upheld, the Applicant contends that the listed claims are allowable by virtue of their dependence on other allowable claims. As this dependence is the sole rationale put forth for the allowability of said dependent claims, the Applicant is directed to the Examiner's remarks above. Additionally, any other arguments the Applicant made that were not specifically addressed in this Office Action appeared to directly rely on an argument presented elsewhere in the Applicant's response that was traversed, rendered moot or found persuasive above.

Conclusion

26. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael B. McFadden whose telephone number is (571)272-8013. The examiner can normally be reached on Monday-Friday 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sam Sough can be reached on (571)272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MBM
03/28/2008

/Hyung SOUGH/
Supervisory Patent Examiner, Art Unit 2188
03/30/08